LINX® TECHNOLOGIES

WIRELESS MADE SIMPLE®

HIGH-PERFORMANCE

RF MODULE

RXM-900-HP3-xxx

HP3 SERIES RECEIVER MODULE DATA GUIDE

DESCRIPTION

The HP3 RF receiver module offers complete compatibility and numerous enhancements over previous generations. The HP3 is designed for the cost-effective, high-performance wireless transfer of analog or digital information in the popular 902-928MHz band. All HP3 Series modules feature eight parallel selectable channels, but versions are also available which add serial selection of 100 channels. To ensure reliable performance, the receiver employs FM / FSK demodulation and an advanced dual-conversion microprocessor-controlled synthesized architecture. The receiver is pin- and footprint-compatible with all previous generations, but its overall physical size has been reduced. Both SMD and pinned packages are available. When paired with an HP3 transmitter, a reliable link is created for transferring analog and digital information up to 1,000 feet. (under optimal conditions). As with all Linx modules, the HP3 requires no tuning or additional RF components (except an antenna), making integration straightforward even for engineers without prior RF experience.

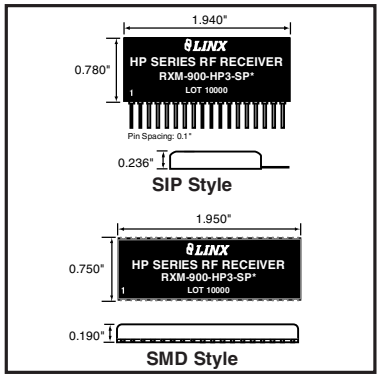


Figure 1: Package Dimensions

FEATURES

- 8 parallel / 100 serial (PS Versions) user-selectable channels
- FM / FSK demodulation for outstanding performance and noise immunity
- Exceptional sensitivity (-100dBm typical)
- Wide-range analog capability including audio (50Hz to 28kHz)
- RSSI and Power-down lines
- Precision frequency synthesized architecture
- No external RF components required
- Compatible with previous HP Series modules
- High data rate (up to 56kbps)
- Wide supply range (2.8 to 13.0VDC)
- Direct serial interface
- Pinned and SMD packages
- Wide temperature range (-30°C to +85°C)

APPLICATIONS INCLUDE

- Wireless Networks / Data Transfer
- Wireless Analog / Audio
- Home / Industrial Automation
- Remote Access / Control
- Remote Monitoring / Telemetry
- Long-Range RFID
- MIDI Links
- Voice / Music / Intercom Links

ORDERING INFORMATION

PART #	DESCRIPTION
RXM-900-HP3-PPO	HP3 Receiver (SIP 8 CH only)
RXM-900-HP3-PPS	HP3 Receiver (SIP 8p / 100s CH)
RXM-900-HP3-SPO	HP3 Receiver (SMD 8 CH only)
RXM-900-HP3-SPS	HP3 Receiver (SMD 8p / 100s CH)
MDEV-900-HP3-PPS-USB	HP3 Development Kit (Pinned Pkg.)
MDEV-900-HP3-PPS-RS232	HP3 Development Kit (Pinned Pkg.)
MDEV-900-HP3-SPS-USB	HP3 Development Kit (SMD Pkg.)
MDEV-900-HP3-SPS-RS232	HP3 Development Kit (SMD Pkg.)
Receivers are supplied in tubes of 10 pcs.	

Revised 1/28/08

ELECTRICAL SPECIFICATIONS

Parameter	Designation	Min.	Typical	Max.	Units	Notes
POWER SUPPLY						
Operating Voltage	V_{CC}	2.8	3.0	13.0	VDC	–
Supply Current	I_{CC}	16.0	19.0	21.0	mA	1
Power-Down Current	I_{PDN}	–	5.6	10.0	µA	2
RECEIVE SECTION						
Receive Frequency Range	F_C	902.62	–	927.62	MHz	3
Center Frequency Accuracy		-50		+50	kHz	
Channel Spacing	–	–	250	–	kHz	3
First IF Frequency		–	34.7	–	MHz	4
Second IF Frequency		–	10.7	–	MHz	4
Noise Bandwidth	N_{3DB}	–	280	–	kHz	–
Data Rate	–	100	–	56,000	bps	–
Analog / Audio Bandwidth	–	50	–	28,000	Hz	4
Analog / Audio Output Level		0.8	1.1	2.0	VAC	5
Data Output:						
Logic Low	–	0.0	–	0.5	VDC	6
Logic High	–	V_{CC}-0.3	–	V_{CC}	VDC	6
Output Impedance		–	17	–	kohms	–
Data Output Source Current		–	230	–	µA	7
Receiver Sensitivity		-94	-100	-107	dBm	8,9
RSSI:						
Dynamic Range		60	70	80	dB	4
Gain		–	24	–	mV/dB	4
Voltage With No Carrier		–	–	1.6	V	4
Spurious Emissions		–	-57	–	dBm	4
Interference Rejection:						
F_C±1MHz		–	54	–	dB	4
F_C±5MHz		–	57	–	dB	4
ANTENNA PORT						
RF Input Impedance	R_{OUT}	–	50	–	Ω	4
TIMING						
Receiver Turn-On Time:						
via V_{CC}	T4	–	–	7.0	mSec	4
via PDN	T3	–	–	3.0	mSec	4
Channel Change Time	T2	–	–	1.5	mSec	4
Max time between transitions	T_1	–	–	20	mSec	4
ENVIRONMENTAL						
Operating Temperature Range	–	-30	–	+85	°C	4

Table 1: HP3 Series Receiver Specifications

Notes

1. Over the entire operating voltage range.
2. With the PDN pin low.
3. Serial mode.
4. Characterized, but not tested.
5. With 1kHz sine wave @ 115kHz transmitter deviation
6. No load.
7. With 1V output drop.
8. For 10^{-5} @ 9,600bps.
9. At specified center frequency.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3	to	+18.0	VDC
Any Input or Output Pin	-0.3	to	V_{CC}	VDC
Operating Temperature	-30	to	+85	°C
Storage Temperature	-45	to	+85	°C
Soldering Temperature	+260°C for 10 seconds			

***NOTE* Exceeding any of the limits of this section may lead to permanent damage to the device. Furthermore, extended operation at these maximum ratings may reduce the life of this device.**

PERFORMANCE DATA

These performance parameters are based on module operation at 25°C from a 3.0VDC supply unless otherwise noted. Figure 2 illustrates the connections necessary for testing and operation. It is recommended all ground pins be connected to the ground plane. The pins marked NC have no electrical connection.

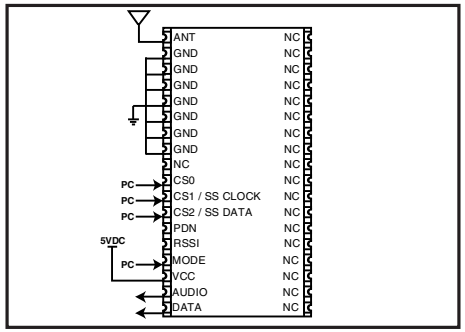


Figure 2: Test / Basic Application Circuit

TYPICAL PERFORMANCE GRAPHS

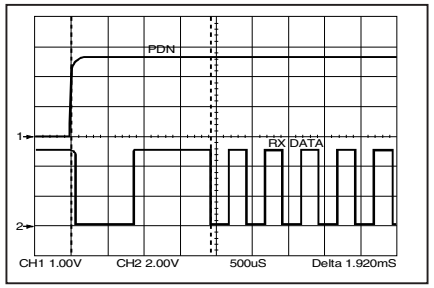


Figure 3: RX Enabled to Valid Data

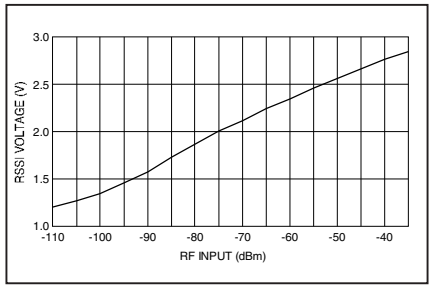


Figure 4: Receiver RSSI

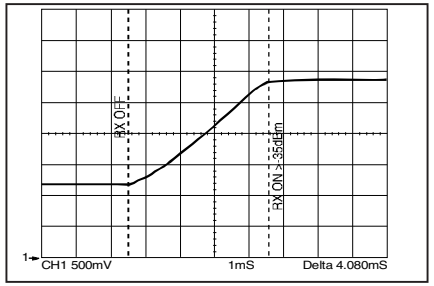


Figure 5: Worst Case RSSI Response Time

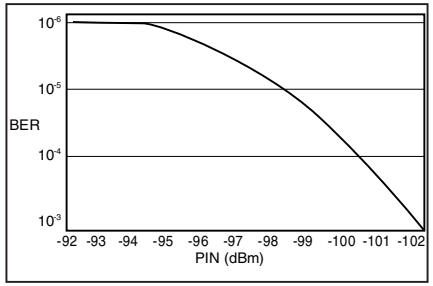


Figure 6: BER vs. Input Power (typical)

PIN ASSIGNMENTS

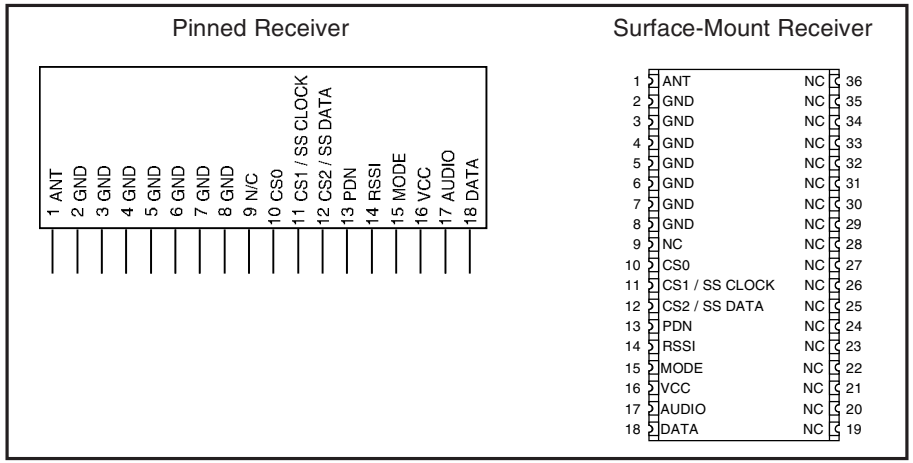


Figure 7: HP3 Series Receiver Pinout

Pin #	Name	Description
1	ANT	50-ohm RF Input
2-8	GND	Analog Ground
9	NC	No Connection
10	CS0	Channel Select 0
11	CS1 / SS CLOCK	Channel Select 1 / Serial Select Clock. Channel Select 1 when in parallel channel selection mode, clock input for serial channel selection mode.
12	CS2 / SS DATA	Channel Select 1 / Serial Select Data. Channel Select 2 when in parallel channel selection mode, data input for serial channel selection mode.
13	PDN	Power Down. Pulling this line low will place the receiver into a low-current state. The module will not be able to receive a signal in this state.
14	RSSI	Received Signal Strength Indicator. This line will supply an analog voltage that is proportional to the strength of the received signal.
15	MODE	Mode Select. GND for parallel channel selection, V_{CC} for serial channel selection
16	V_{CC}	Supply Voltage
17	AUDIO	Recovered Analog Output
18	DATA	Digital Data Output. This line will output the demodulated digital data.
19-36	NC	No Connection (SMD only)

PIN DESCRIPTIONS

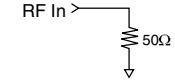
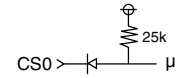
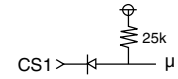
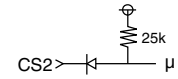
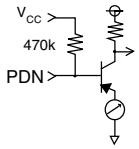
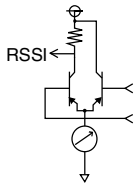
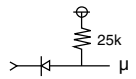
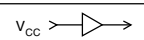
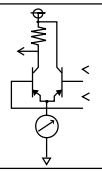
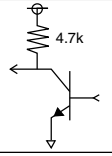
Pin #	Name	Equivalent Circuit	Description
1	ANT		50-ohm RF Input
2-8	GND		Analog Ground
9	NC		No Connection
10	CS0		Channel Select 0
11	CS1 / SS CLOCK		Channel Select 1 / Serial Select Clock
12	CS2 / SS DATA		Channel Select 2 / Serial Select Data
13	PDN		Power Down (Active Low)
14	RSSI		Received Signal Strength Indicator
15	MODE		Mode Select
16	V_{CC}		Voltage Input 2.8-13V
17	AUDIO		$1V_{P-P}$ Analog Output
18	DATA		Digital Data Output
19-36	NC	SMD Only	No Connection

Figure 8: Pin Functions and Equivalent Circuits

THEORY OF OPERATION

The HP3 is a high-performance multi-channel, dual-conversion superhet receiver capable of recovering both analog (FM) and digital (FSK) information from a matching HP Series transmitter. FM / FSK modulation offers significant advantages over AM or OOK modulation methods, including increased noise immunity and the receiver's ability to capture in the presence of multiple signals. This is especially helpful in crowded bands, like that in which the HP3 operates.

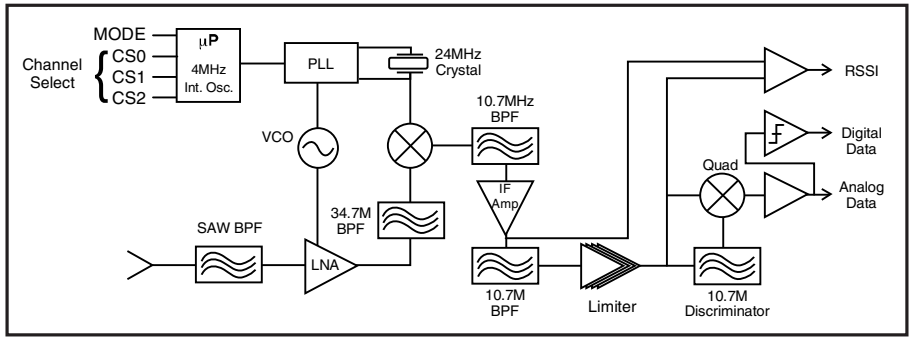


Figure 9: HP3 Series Receiver Block Diagram

The single-ended RF port is matched to 50-ohms to support commonly available antennas, such as those manufactured by Linx. The RF signal coming in from the antenna is filtered by a Surface Acoustic Wave (SAW) filter to attenuate unwanted RF energy. A SAW filter provides significantly higher performance than other filter types, such as an LC bandpass filter.

Once filtered, the signal is amplified by a Low Noise Amplifier (LNA) to increase the receiver sensitivity and lower the overall noise figure of the receiver. After the LNA, the signal is mixed with a synthesized local oscillator operating 34.7MHz below the incoming transmission frequency to produce the first Intermediate Frequency (IF).

The second conversion and FM demodulation is achieved by a high-performance IF strip that mixes the 34.7MHz first conversion frequency with 24.0MHz from a precision crystal oscillator. The resulting second IF of 10.7MHz is then highly amplified in preparation for demodulation.

A quadrature demodulator is used to recover the baseband signal from the carrier. The demodulated waveform is filtered, after which it closely resembles the original signal. The signal is routed to the analog output pin and the data slicer stage, which provides squared digital output via the data output pin. A key feature of the HP3 is the transparency of its digital output, which does not impose balancing or duty-cycle requirements within a range of 100bps to 56kbps.

An on-board microcontroller manages receiver functions and greatly simplifies user interface. The microcontroller reads the channel selection lines and programs the on-board synthesizer. This frees the designer from complex programming requirements and allows for manual or software channel selection. The microcontroller also monitors incoming signal strength and squelches the data output when the signal is not strong enough for accurate data detection.

POWER-UP SEQUENCE

As previously mentioned, the HP3 is controlled by an on-board microprocessor. When power is applied, the microprocessor executes the receiver start-up sequence, after which the receiver is ready to receive valid data.

The adjacent figure shows the start-up sequence. This sequence is executed when power is applied to the V_{CC} line or when the PDN line is taken high.

On power-up, the microprocessor reads the external channel selection lines and sets the frequency synthesizer to the appropriate channel. Once the frequency synthesizer has stabilized, the receiver is ready to accept data.

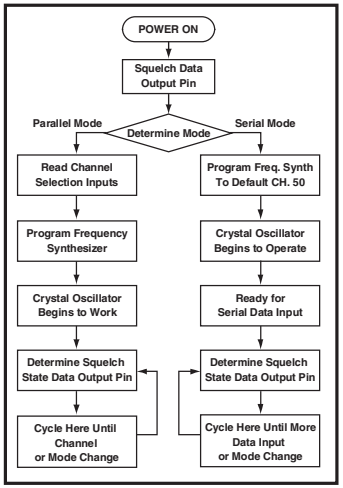


Figure 10: Start-Up Sequence

POWER SUPPLY

The HP3 incorporates a precision, low-dropout regulator on-board, which allows operation over an input voltage range of 2.8 to 13 volts DC. Despite this regulator, it is still important to provide a supply that is free of noise. Power supply noise can significantly affect the receiver sensitivity; therefore, providing a clean power supply for the module should be a high priority during design.

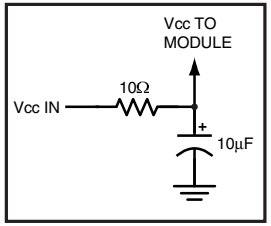


Figure 11: Supply Filter

A 10Ω resistor in series with the supply followed by a 10µF tantalum capacitor from V_{CC} to ground will help in cases where the quality of supply power is poor. This filter should be placed close to the module's supply lines. These values may need to be adjusted depending on the noise present on the supply line.

USING THE PDN PIN

The Power Down (PDN) line can be used to power down the receiver without the need for an external switch. This line has an internal pull-up, so when it is held high or simply left floating, the module will be active.

When the PDN line is pulled to ground, the receiver will enter into a low-current (<10µA) power-down mode. During this time the receiver is off and cannot perform any function. It may be useful to note that the startup time coming out of power-down will be slightly less than when applying V_{CC}.

The PDN line allows easy control of the receiver state from external components, like a microcontroller. By periodically activating the receiver, checking for data, then powering down, the receiver's average current consumption can be greatly reduced, saving power in battery-operated applications.

THE DATA OUTPUT

The DATA line outputs recovered digital data. It is an open collector output with an internal 4.7kΩ pull-up. When an RF transmission is not present, or when the received signal strength is too low to ensure proper demodulation, the data output is squelched continuous high. This feature supports direct operation with UARTs, which require their input to be continuously high. An HP3 transmitter and receiver can be directly connected between two UARTs without the need for buffering or logical inversion. It should be noted that the squelch level is set just over the receiver's internal noise threshold. Any external RF activity above that threshold will "break squelch" and produce hashing on the line. While the DATA line will be reliably squelched in low-noise environments, the designer should always plan for the potential of hashing.

AUDIO OUTPUT

The HP3 Series is optimized for the transmission of serial data; however, it can also be used very effectively to send a variety of analog signals, including audio. The ability of the HP3 to send combinations of audio and data opens new areas of opportunity for creative design.

The analog output of the AUDIO line is valid from 50 Hz to 28 kHz, providing an AC signal of about 1V peak-to-peak. This is a high impedance output and not suitable for directly driving low-impedance loads, such as a speaker. In applications where a low impedance load is to be driven, a buffer circuit should always be used. For example, in the case of a speaker, a simple op-amp circuit such as the one shown below can be used to act as an impedance converter.

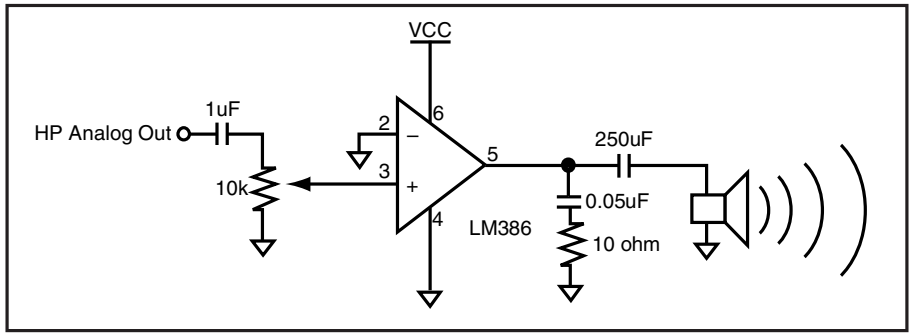


Figure 12: Audio Buffer Amplifier

The transmitter's modulation voltage is critical, since it determines the carrier deviation and distortion. The transmitter input level should be adjusted to achieve the optimum results for your application in your circuit. Please refer to the transmitter data guide for full details.

When used for audio, the analog output of the receiver should be filtered and buffered to obtain maximum sound quality. For voice, a 3-4kHz low-pass filter is often employed. For broader-range sources, such as music, a 12-17kHz cutoff may be more appropriate. In applications that require high-quality audio, a compandor may be used to further improve SNR. The HP3 is capable of providing audio quality comparable to a radio or intercom. For applications where true high fidelity audio is required, the HP3 will probably not be the best choice, and a device optimized for audio should be utilized.

TIMING CONSIDERATIONS

There are four major timing considerations to be aware of when designing with the HP3 Series receiver. These are shown in the table below.

Parameter	Description	Max.
T1	Time between DATA output transitions	20.0mS
T2	Channel change time (time to valid data)	1.5mS
T3	Receiver turn-on time via PDN	3.0mS
T4	Receiver turn-on time via V_{CC}	7.0mS

T1 is the maximum amount of time that can elapse without a data transition. Data must always be considered in both the analog and the digital domain. Because the data stream is asynchronous and no particular format is imposed, it is possible for the data to meet the receiver's data rate requirement yet violate the analog frequency requirements. For example, if a 255 (0FF hex) were sent continuously, the receiver would view the data as a DC level. It would hold that level until a transition was required to meet the minimum frequency specification. If no transition occurred, data integrity could not be guaranteed. While no particular structure or balancing requirement is imposed, the designer must ensure that both analog and digital signals meet the transition specification.

T2 is the worst-case time needed for a powered-up module to switch between channels after a valid channel selection. This time does not include external overhead for loading a desired channel in the serial channel-selection mode.

T3 is the time to receiver readiness from the PDN line going high. Receiver readiness is determined by valid data on the DATA line. This assumes an incoming data stream and the presence of stable supply on V_{CC}.

T4 is the time to receiver readiness from the application of V_{CC}. Receiver readiness is determined by valid data on the DATA line. This assumes an incoming data stream and the PDN line is high or open.

RECEIVING DATA

Once an RF link has been established, the challenge becomes how to effectively transfer data across it. While a properly designed RF link provides reliable data transfer under most conditions, there are still distinct differences from a wired link that must be addressed. Since the modules do not incorporate internal encoding or decoding, the user has tremendous flexibility in how data is handled.

It is important to separate the types of transmissions that are technically possible from those that are legally allowed in the country of operation. Application Notes AN-00126, AN-00140 and Part 15, Section 249 of the FCC rules should be reviewed for details on acceptable transmission content in the U.S.

If you want to transfer simple control or status signals (such as button presses) and your product does not have a microprocessor or you wish to avoid protocol development, consider using an encoder / decoder IC set. These chips are available from several manufacturers, including Linx. They take care of all encoding and decoding functions and provide a number of data lines to which switches can be directly connected. Address bits are usually provided for security and to allow the addressing of multiple receivers independently. These ICs are an excellent way to bring basic remote control products to market quickly and inexpensively. It is also a simple task to interface with inexpensive microprocessors or one of many IR, remote control, DTMF, or modem ICs.

CHANNEL SELECTION

Parallel Selection

All HP3 receiver models feature eight parallel selectable channels. Parallel Mode is selected by grounding the MODE line. In this mode, channel selection is determined by the logic states of pins CS0, CS1, and CS2, as shown in the adjacent table. A '0' represents ground and a '1' the positive supply. The on-board microprocessor performs all PLL loading functions, eliminating external programming and allowing channel selection via DIP switches or a product's processor.

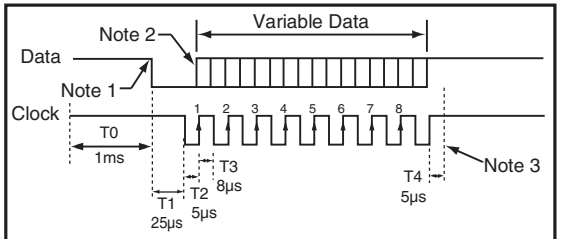
CS2	CS1	CS0	Channel	Frequency
0	0	0	0	903.37
0	0	1	1	906.37
0	1	0	2	907.87
0	1	1	3	909.37
1	0	0	4	912.37
1	0	1	5	915.37
1	1	0	6	919.87
1	1	1	7	921.37

Table 2: Parallel Channel Selection Table

Serial Selection

In addition to the Parallel Mode, PS versions of the HP3 also feature 100 serially selectable channels. The Serial Mode is entered when the MODE line is left open or held high. In this condition, CS1 and CS2 become a synchronous serial port, with CS1 serving as the clock line and CS2 as the data line. The module is easily programmed by sending and latching the binary number (0 to 100) of the desired channel (see the adjacent Serial Channel Selection Table). With no additional effort, the module's microprocessor handles the complex PLL loading functions.

The Serial Mode is straightforward; however, minimum timings and bit order must be followed. Loading is initiated by taking the clock line high and the data line low as shown. The eight-bit channel number is then clocked-in one bit at a time, with the LSB first.



1) Loading begins when clock line is high and data line is taken low
2) Ensure that edge is fully risen prior to high-clock transition
3) Both lines high triggers automatic latch

(T0) Time between packets or prior to data startup .....1mS min.
(T1) Data-LO / Clock-HI to Data-LO / Clock-LO .....25µS min.
(T2) Clock-LO to Clock-HI .....5µS min.
(T3) Clock-HI to Clock-LO .....8µS min.
(T4) Data-HI / Clock-HI .....5µS min.
Total Packet Time .....157µS min.

Figure 13: PLL Serial Data Timing

There is no maximum time for this process, only the minimum times that must be observed. After the eighth bit, both the clock and data lines should be taken high to trigger the automatic data latch. A typical software routine can complete the loading sequence in under 200uS. Sample code is available on the Linx website.

NOTE: When the module is powered up in the Serial Mode, it will default to channel 50 until changed by user software. This allows testing apart from external programming and prevents out-of-band operation. When programmed properly, the dwell time on this default channel can be less than 200uS. Channel 50 is not counted as a usable channel since data errors may occur as transmitters also default to channel 50 on startup. If a loading error occurs, such as a channel number >100 or a timing problem, the receiver will default to serial channel 0. This is useful for debugging as it verifies serial port activity.

SERIAL CHANNEL SELECTION TABLE

CHANNEL	TX FREQUENCY	RX LO	CHANNEL	TX FREQUENCY	RX LO
0	902.62	867.92	51	915.37	880.67
1	902.87	868.17	52	915.62	880.92
2	903.12	868.42	53	915.87	881.17
3	903.37	868.67	54	916.12	881.42
4	903.62	868.92	55	916.37	881.67
5	903.87	869.17	56	916.62	881.92
6	904.12	869.42	57	916.87	882.17
7	904.37	869.67	58	917.12	882.42
8	904.62	869.92	59	917.37	882.67
9	904.87	870.17	60	917.62	882.92
10	905.12	870.42	61	917.87	883.17
11	905.37	870.67	62	918.12	883.42
12	905.62	870.92	63	918.37	883.67
13	905.87	871.17	64	918.62	883.92
14	906.12	871.42	65	918.87	884.17
15	906.37	871.67	66	919.12	884.42
16	906.62	871.92	67	919.37	884.67
17	906.87	872.17	68	919.62	884.92
18	907.12	872.42	69	919.87	885.17
19	907.37	872.67	70	920.12	885.42
20	907.62	872.92	71	920.37	885.67
21	907.87	873.17	72	920.62	885.92
22	908.12	873.42	73	920.87	886.17
23	908.37	873.67	74	921.12	886.42
24	908.62	873.92	75	921.37	886.67
25	908.87	874.17	76	921.62	886.92
26	909.12	874.42	77	921.87	887.17
27	909.37	874.67	78	922.12	887.42
28	909.62	874.92	79	922.37	887.67
29	909.87	875.17	80	922.62	887.92
30	910.12	875.42	81	922.87	888.17
31	910.37	875.67	82	923.12	888.42
32	910.62	875.92	83	923.37	888.67
33	910.87	876.17	84	923.62	888.92
34	911.12	876.42	85	923.87	889.17
35	911.37	876.67	86	924.12	889.42
36	911.62	876.92	87	924.37	889.67
37	911.87	877.17	88	924.62	889.92
38	912.12	877.42	89	924.87	890.17
39	912.37	877.67	90	925.12	890.42
40	912.62	877.92	91	925.37	890.67
41	912.87	878.17	92	925.62	890.92
42	913.12	878.42	93	925.87	891.17
43	913.37	878.67	94	926.12	891.42
44	913.62	878.92	95	926.37	891.67
45	913.87	879.17	96	926.62	891.92
46	914.12	879.42	97	926.87	892.17
47	914.37	879.67	98	927.12	892.42
48	914.62	879.92	99	927.37	892.67
49	914.87	880.17	100	927.62	892.92
50*	915.12	880.42	= Also available in Parallel Mode		

**See NOTE on previous page.*

PROTOCOL GUIDELINES

While many RF solutions impose data formatting and balancing requirements, Linx RF modules do not encode or packetize the signal content in any manner. The received signal will be affected by such factors as noise, edge jitter, and interference, but it is not purposefully manipulated or altered by the modules. This gives the designer tremendous flexibility for protocol design and interface.

Despite this transparency and ease of use, it must be recognized that there are distinct differences between a wired and a wireless environment. Issues such as interference and contention must be understood and allowed for in the design process. To learn more about protocol considerations, we suggest you read Linx Application Note AN-00160.

Errors from interference or changing signal conditions can cause corruption of the data packet, so it is generally wise to structure the data being sent into small packets. This allows errors to be managed without affecting large amounts of data. A simple checksum or CRC could be used for basic error detection. Once an error is detected, the protocol designer may wish to simply discard the corrupt data or implement a more sophisticated scheme to correct it.

INTERFERENCE CONSIDERATIONS

The RF spectrum is crowded and the potential for conflict with other unwanted sources of RF is very real. While all RF products are at risk from interference, its effects can be minimized by better understanding its characteristics.

Interference may come from internal or external sources. The first step is to eliminate interference from noise sources on the board. This means paying careful attention to layout, grounding, filtering, and bypassing in order to eliminate all radiated and conducted interference paths. For many products, this is straightforward; however, products containing components such as switching power supplies, motors, crystals, and other potential sources of noise must be approached with care. Comparing your own design with a Linx evaluation board can help to determine if and at what level design-specific interference is present.

External interference can manifest itself in a variety of ways. Low-level interference will produce noise and hashing on the output and reduce the link's overall range.

High-level interference is caused by nearby products sharing the same frequency or from near-band high-power devices. It can even come from your own products if more than one transmitter is active in the same area. It is important to remember that only one transmitter at a time can occupy a frequency, regardless of the coding of the transmitted signal. This type of interference is less common than those mentioned previously, but in severe cases it can prevent all useful function of the affected device.

Although technically it is not interference, multipath is also a factor to be understood. Multipath is a term used to refer to the signal cancellation effects that occur when RF waves arrive at the receiver in different phase relationships. This effect is a particularly significant factor in interior environments where objects provide many different signal reflection paths. Multipath cancellation results in lowered signal levels at the receiver and, thus, shorter useful distances for the link.

TYPICAL APPLICATIONS

The figure below shows a typical RS-232 circuit using the HP3 Series receiver and a Maxim MAX232. The receiver outputs a serial data stream and the MAX232 converts that to RS-232 compliant signals. The MODE line is grounded so the channels are selected by the DIP switches.

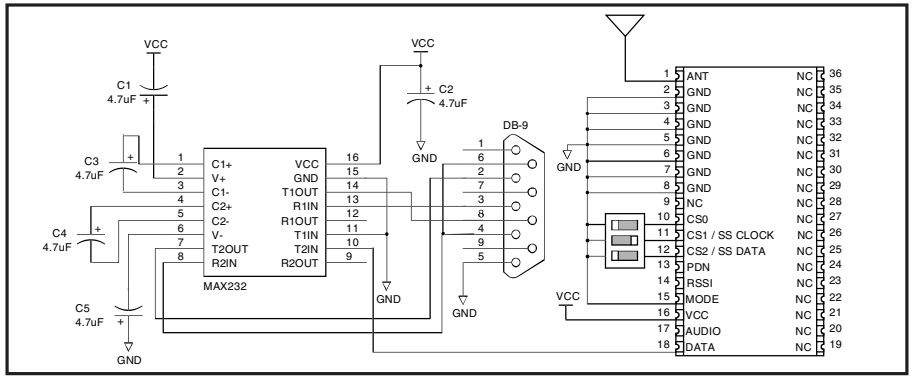


Figure 14: HP3 Receiver and MAX232 IC

The figure below shows a circuit using the QS Series USB module. The QS converts the data from the receiver into USB compliant signals to be sent to a PC. The MODE line is high, so the module is in Serial Channel Select mode. The RTS and DTR lines are used to load the channels. Application Note AN-00155 shows sample source code that can be adapted to use on a PC. The QS Series Data Guide and Application Note AN-00200 discuss the hardware and software set-up required for QS Series modules.

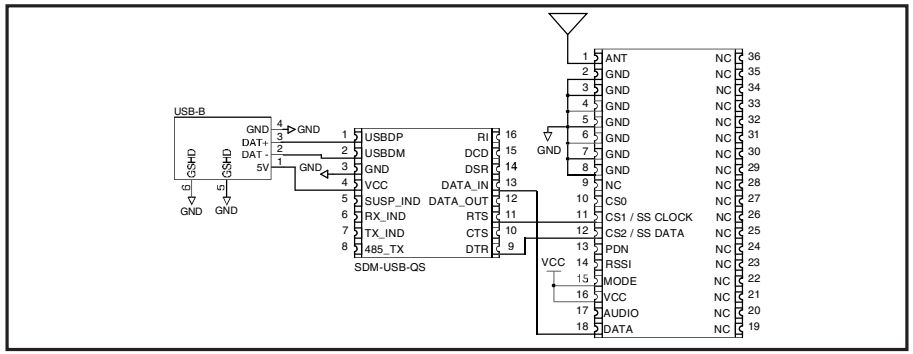


Figure 15: HP3 Receiver and Linx QS Series USB Module

The receiver can also be connected to a microcontroller, which will interpret the data and take specific actions. A UART may be employed or an I / O line may be used to continuously monitor the DATA line for a valid packet. The receiver may be connected directly to the microcontroller without the need for buffering or amplification.